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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,242	01/23/2002	Bo Chang	CYPR-PM01007	7803

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EXAMINER	
LAIR, DONALD M	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,242	CHANG ET AL.	
	Examiner	Art Unit	
	Donald M. Lair	2858	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,8 and 38-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8 and 38-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4, 8 and 38 – 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Fogal et al. (US-6,117,693).

3. In regards to Claims 1 and 38, Fogal et al. discloses a method for testing wire bonds in an integrated circuit package, comprising:

receiving a die comprising an integrated circuit formed on a semiconductor substrate (Column 3, lines 27 – 36);

forming a wire connection between a circuit contact pad in said integrated circuit and a lead contact pad in a package substrate bonded to said semiconductor substrate (Fig. 4, elements 32);

testing said wire connection for non-stick failure by checking for electrical continuity along a path comprising said circuit contact pad and a non-stick detection (NSD) contact pad coupled to said semiconductor substrate, wherein said semiconductor substrate itself provides electrical continuity between said circuit contact pad and said NSD contact pad for said testing. This embodiment is shown at Figure 2, wherein the NSD contact pads are the contact pads 20 that are connected to conductors 16 and contacts 30.

4. In regards to Claim 42, Fogal et al. discloses a method for testing wire bonds in an integrated circuit package comprising:

connecting the first end of a length of a wire fed from a wire spool (Column 6, lines 12 – 17) to a circuit contact pad in an integrated circuit formed on a semiconductor substrate (Figs. 1, 3B and 4); and

testing said connecting of said first end of said wire to said circuit contact pad for non-stick failure by checking for electrical continuity on a path comprising, in order, said wire spool (Column 6, lines 12 – 17), said length of wire (Fig. 4, element 32), said circuit contact pad (Figs. 2 and 4, element 20), said semiconductor substrate (Fig. 4, element 12), and a non-stick detection contact pad coupled to said semiconductor substrate (Fig. 2, element 20 as applied to claims 1 and 38), wherein said semiconductor substrate provides electrical continuity between said circuit contact pad and said NSD contact pad for said testing, wherein non-stick failure at said first end is indicated if said electrical continuity does not exist (Column 2, lines 16 – 28).

5. In regards to Claim 4, Fogal et al. discloses the method described above, wherein said lead contact pad is electrically isolated from other lead contact pads in said package substrate (Figs. 2 and 4, element 14).

6. In regards to Claim 8, Fogal et al. discloses the method described above, wherein the method is performed recursively for a plurality of wire connections (Fig. 2).

7. In regards to Claims 39 and 43, Fogal et al. discloses the method described above, wherein said integrated circuit die is bonded to a package substrate (Figs. 1, 2, 4 and 4a; Column 2, lines 8 – 15).

8. In regards to Claims 40 and 44, Fogal et al. discloses the method described above, wherein said NSD contact pad extends through said package substrate and is coupled via a trace line to a bus line that is coupled to a grounded mold gate, wherein said path for checking electrical continuity further comprises said trace line, said bus line and said mold gate (Fig. 2, elements 26, 30 and 38).

9. In regards to Claim 41, Fogal et al. discloses the method described above, wherein said wire is fed from a wire spool and wherein said path for checking electrical continuity further comprises said wire and said wire spool (Column 6, lines 12 – 27).

10. In regards to Claim 45, Fogal et al. discloses the method described above, further comprising:

connecting the second end of said length o wire to a lead contact pad in said package substrate, wherein successful connection of said second end to said lead contact pad causes said length of wire to separate from said wire spool (Column 6, lines 7 – 17); and

testing connection of said second end to said lead contact pad for non-stick failure by checking for electrical continuity along said path, wherein non-stick failure at said second end is indicated if electrical continuity exists (Column 2, lines 16 – 28; Column 6, lines 18 – 27).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fogal et al. in view of Brooks et al. (US-6,326,244).

13. In regards to Claim 3, Fogal et al. discloses the method of testing described above, but fails to teach how the integrated circuit die is bonded to the package substrate.

14. Brooks et al. teaches using electrically non-conductive, thermally conductive epoxy to bond the integrated circuit die to the package substrate (Column 7, lines 21 – 35).

15. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method disclosed by Fogal et al. by using an electrically non-conductive epoxy to bond the integrated circuit die to the package substrate, as taught by Brooks et al., for the purpose of protecting the package components.

16. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fogal et al. in view of Gang (US-6,566,168).

17. In regards to Claim 2, Fogal et al. discloses the method of testing described above, but fails to teach how the integrated circuit die is bonded to the package substrate.

18. Gang teaches using electrically conductive epoxy to bond the integrated circuit die to the package substrate (Column 3, lines 55 – 64).

19. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method disclosed by Fogal et al. by using an electrically conductive epoxy to bond the integrated circuit die to the package substrate, as taught by Gang, for the purpose of connecting the circuit die to the package substrate.

Response to Arguments

20. Applicant's arguments with respect to claims 1-4 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donald M. Lair whose telephone number is (571) 272-2232. The examiner can normally be reached on Monday - Friday, 8 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on (571) 272-2233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donald M. Lair
Patent Examiner
Art Unit 2858
June 8, 2004

ANJAN DEB
PRIMARY EXAMINER